

REMARKS

Claims 1-20 remain pending. Claims 1, 9, and 18 have been amended.

Claim 21 has been added. No new matter has been added.

35 U.S.C. Section 102 Rejections

Paragraph 3 of the above referenced Office Action rejects independent Claims 1, 9, and 18 as being anticipated by Moreno (US 6,678,795). As such, Applicants respectfully traverse and assert that the independent Claims 1, 9, and 18 are not anticipated or rendered obvious by Moreno.

Applicants direct the Examiner to currently amended Claim 9 which recites in part (emphasis added):

a cache memory coupled to the prefetch unit, wherein the prefetch unit uses a bit vector to predictively load target cache lines from the system memory into the cache memory to reduce an access latency of the processor, and wherein the target cache lines are indicated by the stream type sequential access pattern identified by the trackers.

Independent Claim 1 and 18 recite distinguishing limitations similar to those recited in Claim 9.

Applicants respectfully assert that Moreno does not teach or suggest embodiments of the present invention as recited in Claim 9. Applicants point out that paragraph 5 of the above referenced Office Action states that Moreno does not specifically teach that these accesses are consecutive (Page 7).

Further, Applicants point out that a previous Office Action (mailed

12/18/2006) states Moreno does not specifically disclose that the order of previous accesses to the two cache lines was not interrupted by other cache line accesses (Page 4).

Further, to the extent that Moreno may mention that upon a miss to the first memory from the at least one processor based on a request a table is searched and misses corresponding to entries result in prefetch requests (Col 2, lines 21-26), Applicants respectfully assert that Moreno does not teach or suggest predictively loading target cache lines based on stream type sequential access, as claimed. More specifically, Applicants understand Moreno to generate prefetch requests based on misses (Col 2, lines 21-26). Applicants respectfully assert that prefetch requests based on misses is substantially different from predictively prefetching cache lines based on stream type sequential accesses, as claimed (emphasis added). Moreover, Applicants respectfully point out the cited portions of Moreno describe prefetching of arbitrary lines within a page, which do not need to exhibit any pattern (Col 2, lines 1-2).

Accordingly, Applicants respectfully asset that Moreno does not anticipate Claim 9 within the meaning of 35 U.S.C. §102(e) nor does Moreno render Claim 9 obvious within the meaning of 35 U.S.C. §103(a).

Independent Claims 1 and 18 are patentable for similar reasons. Dependent claims are patentable by virtue of their dependency.

35 U.S.C. Section 103 Rejections

Paragraph 5 of the above referenced Office Action rejects dependent Claims 4, 12, and 20 as being rendered obvious by Moreno (US 6,678,795). For the reasons stated above, Applicants respectfully assert that independents Claim 1, 9, and 18 are allowable over Moreno. As such, Applicants respectfully assert that Claims 4, 12 and 20 are not rendered obvious by Moreno by virtue of their dependency. Further, the rejection states that Moreno does not specifically teach these accesses are consecutive. To extent that Figure 1 of Moreno may mention adjacent cache lines accesses in a bucket (Figure 1), Applicants respectfully assert that Figure 1 does not show the order of the cache line accesses in a bucket (emphasis added). Thus, Applicants respectfully assert that Figure 1 of Moreno does not teach or suggest the features of consecutive accesses, as claimed, as recited in Claim 4. Claims 12 and 20 recite distinguishing limitations similar to those recited in Claim 4. Therefore, Applicants respectfully assert that embodiments as recited by Claims 4, 12, and 20 are not rendered obvious by Moreno.

Claims 16, 17, and 19 stand rejected as being unpatentable over Moreno in view of Bittel (US 6,820,173), Microsoft Computer Dictionary, and Brooks (US 6,081,868) respectively.

Concerning Claim 16, the rejection relies on Bittel teaching a prefetch apparatus comprising a prefetch unit and a cache memory within the prefetch unit. Applicants respectfully disagree. For the reasons stated above, Applicant respectfully submits that independent Claim 9, from which Claim 16 depends is allowable over Moreno. In addition, Applicants respectfully submit that Bittel does not remedy the shortcomings of Moreno. More specifically, Applicants respectfully assert that Bittel does not teach or suggest predictively loading target cache lines based on stream type sequential access, as claimed. Therefore, Applicants respectfully assert that the embodiments of the present invention as recited in Claim 16 are not rendered obvious by the combination of Moreno and Bittel within the meaning of 35 U.S.C. 103(a).

Concerning Claim 17, the above referenced Office Action rejects Claim under 35 U.S.C. 103(a) as being unpatentable over Moreno further in view of Microsoft Computer Dictionary (hereinafter “Microsoft”). Applicants respectfully disagree. For the reasons stated above, Applicant respectfully submits that independent Claim 9, from which Claim 17 depends is allowable

over Moreno. In addition, Applicants respectfully submit that Microsoft does not remedy the shortcomings of Moreno. More specifically, Applicants respectfully assert that Microsoft does not teach or suggest predictively loading target cache lines based on stream type sequential access, as claimed. Therefore, Applicants respectfully assert that the embodiments of the present invention as recited in Claim 17 are not rendered obvious by the combination of Moreno and Microsoft within the meaning of 35 U.S.C. 103(a).

Concerning Claim 19, the above referenced Office Action rejects Claim under 35 U.S.C. 103(a) as being unpatentable over Moreno further in view of Brooks (US 6,081,868). Applicants respectfully disagree. For the reasons stated above, Applicant respectfully submits that independent Claim 18, from which Claim 19 depends is allowable over Moreno. In addition, Applicants respectfully submit that Brooks does not remedy the shortcomings of Moreno. More specifically, Applicants respectfully assert that Brooks does not teach or suggest predictively loading target cache lines based on stream type sequential access, as claimed. Therefore, Applicants respectfully assert that the embodiments of the present invention as recited in Claim 17 are not rendered obvious by the combination of Moreno and Brooks within the meaning of 35 U.S.C. 103(a).

Therefore, Applicants respectfully submit that Claims 16, 17, and 19 are allowable over Moreno in view of Bittel, Microsoft Computer Dictionary, and Brooks, respectively, as being dependent on allowable base claims.

CONCLUSION

The Examiner is urged to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application. Please charge any additional fees or apply any credits to our PTO deposit account number: 50-4160.

Respectfully submitted,
MURABITO, HAO & BARNES

Dated: 9/23, 2008

/Michael D. Sochor/
Michael D. Sochor
Registration No. 58,348

Two North Market Street
Third Floor
San Jose, CA 95113
(408) 938-9060